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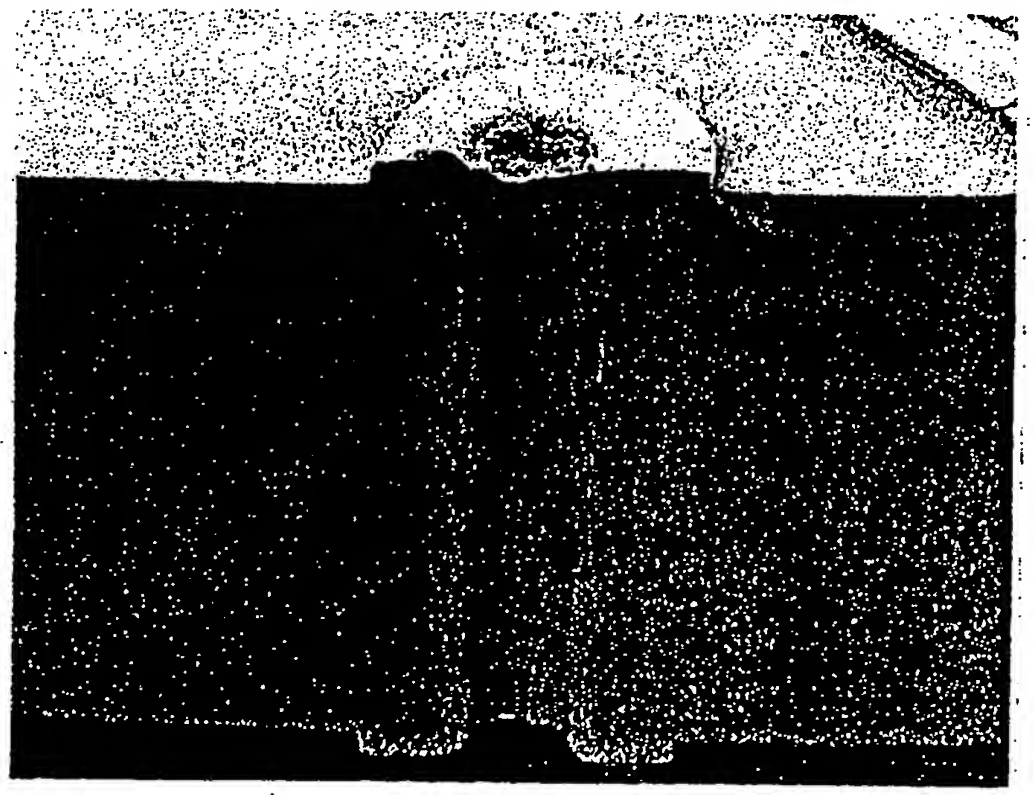

(57) Abstract

A method of forming one or more plugs in a circuit board layer or assembly is described which includes providing the circuit board layer or assembly having a first surface, a second surface, and defining a via containing a plug material in a volatile solvent, evaporating the volatile solvent, and curing the plug material. A product made according to the above method is also described. Also described is a method of forming a partially filled via in a circuit board layer and a method of forming a thermally conductive plug in a circuit board layer for the transfer of thermal energy from one surface of the circuit board to the other.

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FORMING PLUGS IN VIAS OF CIRCUIT BOARD LAYERS AND SUBASSEMBLIES

Related Applications

This application is a continuation-in-part of copending U.S. Patent Application Serial No. 09/159,429, filed September 24, 1998, and also claims the benefit of copending U.S. Provisional Patent Application Serial No. 60/098,819, filed September 2, 1998, the entire disclosure of which is incorporated by reference herein.

Field of the Invention

The present invention relates generally to circuit board layers, and more specifically to a method and apparatus for forming plugs in one or more vias defined by a circuit board layer, and the product obtained using this method.

Background of the Invention

Circuit board through-holes are commonly plated or filled with conductive material in order to provide for the transfer of electrical signals from one surface of the circuit board layer to a second surface of the circuit board layer.

Filled through-holes are typically through-holes which receive contacts or pins of some element external to the circuit board. The through-holes typically are filled manually with a molten conductive material, to both physically and electrically connect the external element to the circuit board. It is also known to form a plug in the through-holes by a method which includes filling the through-holes with a first layer of conductive material, curing this layer, planarizing the circuit board layer to remove the conductive material cured to the surface of the circuit board layer, filling the through-holes with a second conductive material, and curing this second material. Both of these methods are time-consuming and expensive. Furthermore, not only does the latter method require several filling steps, but it also involves a substantial alteration of the surface of the circuit board layer in order to remove the conductive material that is cured onto the surface of the circuit board layer.

Plated through-holes generally involve electroless copper plating which is expensive and coats only the inside surface of the through-holes. It is known to form a thin meniscus of non-

conductive or dielectric material within a via plated with conductive material using a screen without a stencil. This typically is done to allow vacuum hold down of circuit boards for testing, or to prevent assembly materials from propagating from one side of the circuit board to the other, but may be done for other reasons as well. However, the meniscus formed is susceptible to corrosion, thus decreasing the yield of acceptable circuit boards and increasing their cost.

Furthermore, methods of forming plugs in circuit board layers which result in significant alteration of the surfaces of circuit board layer is a disadvantage, particularly if it is desirable to print the circuit board prior to plug formation.

A problem encountered with sequential lamination, as well as lamination in general, is resin loss during lamination. Resin loss is problematic as lost resin present on the surface of the laminate will cure to the outer surfaces of the laminate. Further, resin loss may result in insufficient lamination of the layers. Also, loss of resin into vias may result in a dimpled laminate surface over the via, due to the loss of resin in that area.

In sequential lamination of printed circuit board subassemblies, resin loss typically is reduced by placing rubber pads against the outer layers of the subassemblies during lamination in order to stop resin flow to the outer surfaces of the subassemblies. One disadvantage to this approach is that resin still flows into the vias and, in some cases, results in unsatisfactory bonding between the subassemblies.

Therefore, there exists a need in the art for a method and apparatus to quickly and efficiently form plugs in circuit board through-holes at an acceptable yield and cost. There is a further need for a method of forming plugs in circuit board through-holes without significantly altering either surface of the circuit board layer. Finally, there exists a need in the art for a method to provide a plug with minimal voids formed therein.

Summary of the Invention

This invention provides a novel method and apparatus for forming plugs in vias of a circuit board layer, and the novel product produced by this novel method.

In one aspect, the present invention provides a novel method of forming one or more plugs in a circuit board layer. First, a circuit board layer is provided, the circuit board layer having a first surface, a second surface, and defining a via containing a plug material in a volatile

solvent. The volatile solvent is then evaporated. This may be accomplished at a controlled rate so that the presence of voids in the resulting plug is minimized. In one embodiment, plug material present on the first surface and the second surface of the circuit board layer is substantially removed without causing a significant alteration of either surface of the circuit board layer. Finally, the plug material is cured to form a plug contained within the via defined by the circuit board layer in the case of a conductive plug, or defined by the plated circuit board layer in the case of a non-conductive plug.

In another aspect, the circuit board layer including the plug formed therein is described in terms of the novel method described above.

In yet another aspect, the present invention provides a novel apparatus for filling the one or more of a plurality of vias formed in a circuit board layer. This apparatus is called a fixture and it includes a planar template and an air permeable layer. The template has a first surface, a second surface, and defines one or more through-holes corresponding in position to the one or more vias defined by the circuit board layer. The air permeable layer is disposed on the second surface of the template. In a preferred embodiment, this air permeable layer is substantially impermeable to the plug material so that the plug material is substantially contained within the fixture.

In yet another aspect, the present invention provides a novel method of forming a subassembly comprising a circuit board layer, the circuit board layer having one or more plugs formed therein. First, a circuit board layer is provided, the circuit board layer having a first surface and a second surface, and defining a via containing a plug material in a volatile solvent. The volatile solvent is then evaporated and the plug material cured. Finally, the circuit board layer is laminated to two sheets of conductive material with two intermediate layers of prepreg material.

In another aspect, the subasssembly and a printed circuit board including the subassembly is described in terms of the novel method described above.

In yet another aspect, the present invention provides a novel method of forming one or more plugs in a subassembly for use in a printed circuit board. First, a subassembly is provided. The subassembly includes a circuit board layer laminated to two sheets of conductive material

with two intermediate sheets of prepreg material. A via is formed in the circuit board laminate, the via is plated, and then the via is filled with a plug material in a volatile solvent. The volatile solvent is evaporated and finally the plug material is cured.

In another aspect, a subassembly and a printed circuit board including the subassembly formed therein are described in terms of the novel method described above.

In yet another aspect, the present invention provides a novel method of forming a circuit board layer with a partially filled via. First a circuit board layer is provided that includes a first surface, a second surface, and defines a via. A portion of the via is filled with a plug material in a volatile solvent. The volatile solvent is evaporated and the plug material is then cured to form a partially filled via.

In another aspect, a printed circuit board and a circuit board including the partially filled via formed therein is described in terms of the novel method described above.

In yet another aspect, the present invention provides a novel method of forming a circuit board layer comprising a thermally conductive plug for transfer of thermal energy from a first surface of the circuit board layer to a second surface of the circuit board layer. First, a circuit board layer is provided that has a first surface, a second surface, and defines a via containing a thermally conductive plug material in a volatile solvent. The volatile solvent is evaporated and the thermally conductive plug material is cured.

In another aspect, a printed circuit board and a circuit board layer including the thermally conductive plug formed therein is described in terms of the novel method described above.

Brief Description of the Drawings

The invention is pointed out with particularity in the appended claims. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. The advantages of the invention described above, as well as further advantages of the invention, may be better understood by reference to the following description taken in conjunction with the accompanying drawings, in which:

Figure 1 is a flowchart diagram illustrating an embodiment of a method of forming one or more plugs in a circuit board layer in accordance with the present invention;

Figure 2 is a flowchart diagram illustrating another embodiment of a method of forming one or more plugs in a circuit board layer in accordance with the present invention;

Figure 3 is a schematic perspective cross-sectional view of an embodiment of a circuit board layer with a conductive plug formed in a via defined by the circuit board layer in accordance with the present invention;

Figure 4 is a schematic perspective cross-sectional view of an embodiment of a circuit board layer with a non-conductive plug formed in a plated via defined by the circuit board layer in accordance with the present invention;

Figure 5 is a schematic cross-sectional side view of an embodiment of an apparatus, a stencil, and a circuit board layer in accordance with the present invention;

Figure 6 is a flowchart diagram illustrating a method of forming a subassembly comprising a circuit board layer, the circuit board layer having one or more plugs formed therein, in accordance with the present invention;

Figure 7 is a schematic perspective cross-sectional view of an embodiment of a subassembly comprising a circuit board layer, the circuit board layer having one or more plugs formed therein, in accordance with the present invention;

Figure 8 is a flowchart diagram illustrating a method of forming a subassembly having one or more plugs formed therein in accordance with the present invention;

Figure 9 is a schematic perspective cross-sectional view of an embodiment of a subassembly having one or more plugs formed therein in accordance with the present invention;

Figure 10 is a flowchart diagram illustrating a method of forming a partially filled via in a circuit board layer in accordance with the present invention;

Figure 11 is a perspective cross-sectional photograph of an embodiment of a circuit board layer with a partially filled via in accordance with the present invention; and

Figure 12 is a flowchart diagram illustrating a method of forming a circuit board layer having a thermally conductive plug in accordance with the present invention.

Detailed Description of Preferred Embodiments

In order to more clearly and concisely describe the subject matter of the claims, the following definitions are intended to provide guidance as to the meaning of specific terms used in the following written description, examples and appended claims.

As used herein the term "via" means a through-hole formed in a circuit board layer. Vias are commonly used for the transfer of electrical signals from one side of a circuit board layer to the other side by plating the side walls of the via or filling the via with a conductive material.

As used herein the term "conductive material" means any material that includes a substance that is capable of transmitting electrical signals. As used herein the term "non-conductive material" or "dielectric material" means any material that is not capable of transmitting electrical signals. The term "thermally conductive material," as used herein, means any material that includes a substance that is capable of transmitting thermal energy.

Figure 1 is a flowchart diagram illustrating a method of forming one or more plugs in a circuit board layer. The method includes, in overview, of: providing the printed circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via containing a plug material in a volatile solvent (step 10); evaporating the volatile solvent (step 12); and curing the plug material (step 14).

In step 10 a circuit board layer is provided. The circuit board may be a double sided, multilayer or rigid-flex circuit board. The circuit board may be printed or unprinted. The circuit board layer defines one or more vias containing a plug material in a volatile solvent. The plug material preferably is a polymer based thermoset or thermoplastic and may be conductive or non-conductive. Compounds such as solder masks, for example, HYSOL® SR1000 or HYSOL® SR1010 solder masks made by Dexter Corporation, which have a viscosity of about 30,000 centipoise (cP), are suitable for use as a non-conductive material. Polymer-based plug material, such as SD2361 made by Lackerwerke Peters having a viscosity of from about 26,000 to about 37,000 cP, is suitable for use as a non-conductive material. Polymer-based compounds such as CB100 made by DuPont, Inc. are also suitable for conductive material. These materials and other materials suitable for use in the present invention include solid plug materials dispersed in a volatile solvent. Other equivalent substances would also be suitable and are known in the art.

In step 12, the volatile solvent is evaporated from the conductive material. Preferably, the solvent is evaporated at a controlled rate, below the cure temperature of the plug material, such that the creation of voids in the plug material is minimized. The rate of evaporation also is controlled by drying at a temperature high enough to drive off the volatile solvent without bubble formation. That is, it is preferred that the volatile solvent bleeds out of the plug material with minimal bubble formation. If bubbles are formed in the plug material, during the cure, or other subsequent steps in which the circuit board is exposed to high temperatures, any air or solvent trapped in the voids may expand and cause the material surrounding the void to crack, break, or in extreme cases, explode. The solvent may be evaporated at a temperature from about 40°C to about 100°C, and preferably from about 60°C to about 90°C. The most preferred temperature for each plug material will vary depending on the volatile solvent used therein. The plug material may be dried for about 30 minutes to about 90 minutes, preferably for about 45 minutes to about 75 minutes and most preferably for about 60 minutes, and will vary depending on the drying temperature and the amount of volatile solvent in the plug material. After the solvent is evaporated, the plug material is left in a solid state. Drying the plug material prior to curing minimizes void formation due to the evaporation of solvent during the cure. It also allows for easy removal of excess plug material prior to the cure.

Finally, in step 14 the plug material is cured. The cure temperature is typically in the range of from about 130°C to about 180°C degrees, more preferably between about 150°C and about 170°F, and will vary depending on the chemistry of the material used. The optimal cure temperature for a particular material is typically supplied to the user by the manufacturer of the material. The plug material should be cured for about 30 minutes to about 90 minutes, preferably for about 60 minutes.

Figure 2 is a flowchart diagram illustrating another embodiment of a method of forming one or more plugs in a circuit board layer in accordance with the present invention. The method includes, in overview, the initial steps of: providing the printed circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via (step 16); and deciding whether or not to plate the via (step 18). If the via is to be plated, then the remainder of the method includes: plating the via (step 20); filling the via with a non-conductive plug material in a volatile solvent (step 22); evaporating the volatile solvent (step 24); removing any excess plug

material from both the first surface and the second surface of the circuit board layer (step 26); and curing the plug material (step 28). If the decision is made not to plate the via, then the remainder of the method includes: filling the via with a conductive plug material in a volatile solvent (step 30); evaporating the volatile solvent (step 32); removing any excess plug material from both the first surface and the second surface of the circuit board layer (step 34); and curing the plug material (step 36).

In step 16 a circuit board layer defining a via is provided. As in Figure 1, the circuit board may be a double sided, multilayer or rigid-flex circuit board. The circuit board may be printed or unprinted. The circuit board layer defines one or more vias which may be drilled, etched or punched into the circuit board layer.

In step 18 a decision is made as to whether or not to plate the via. This will depend on various factors including the relative cost and thermal properties of the non-conductive plug material, the plating, and the conductive plug material.

If the decision is made to plate the via, the next step (step 20) is to plate the via with a conductive material. Typically the via is plated with copper, but other conductive materials may also be used. Methods of plating are well known in the art. The plated via is then filled with non-conductive plug material in a volatile solvent (step 22). Compounds such as solder masks, for example, HYSOL® SR1000 or HYSOL® SR1010 solder masks, made by Dexter, which have a viscosity of about 30,000 cP, are suitable for use as a non-conductive material.

The volatile solvent in the plug material is then evaporated (step 24) at a controlled rate as described in connection with step 12 of Figure 1. One advantage of the evaporation step (step 24) is that if this is done at a controlled rate, voids in the plug may be minimized. The evaporation step (step 24) represents a further advantage in that any plug material present on the surfaces of the circuit board from the filling step (step 22), is also dried in the evaporation step (step 24) and may be removed from the surfaces of the circuit board layer without a significant alteration of the surfaces (step 26). Significant alteration occurs, for example, when a conductive trace or portion of a conductive trace printed on the surface of the printed circuit board is removed from the surface of the circuit board layer. When excess plug material is cured to a surface of the circuit board layer, it is typically necessary to significantly alter any traces printed

upon the surface, in order to remove the cured plug material. Significant alteration is not necessary with the present invention, because any dried plug material present on the surfaces is easily removed by brushing or wiping it from the surfaces. Thus, if the circuit board layer provided in step 16 is a printed circuit board layer, the plugs may be formed according to this method without destruction of the printed traces.

A nylon brush may be used to remove this excess material from one or both surfaces of the circuit board layer in step 26 without significantly altering the surfaces. For example, if a 1.2 mil trace is laid down upon a surface of the circuit board layer, a nylon roller brush will typically remove only about 0.1 mil of trace material from the surface of the trace, thus leaving a 1.1 mil trace. This alteration is not substantial and is consistent with other surface preparation methods commonly used in circuit board manufacturing processes. Alternatively, the surfaces may be wiped clean of excess plug material.

It is preferred that substantially all of plug material be removed from the surface of the circuit board layer prior to curing the plug material (step 28), so that the plug material is not cured onto the surface of the circuit board layer and thus difficult to remove without significantly altering or planarizing the surface of the circuit board layer. Another advantage of this method is that in removing the excess plug material from the surfaces (step 26), the surface of the plug itself is planarized. This is desirable because often external components will be placed directly over filled vias and, if there is any bulge or bump in the via, the external component will not sit firmly onto its mounting pad or pads creating the potential for dislocation of the component or defective soldering. Finally, the plug material is cured (step 28) as described above in step 14 of Figure 1 to form a plug contained within the plated via.

If the decision is made not to plate the via, the next step is filling the via with a conductive plug material in a volatile solvent (step 30). As in Figure 1, any conductive compound may be used including polymer-based compounds, such as CB100 made by DuPont, Inc.

The remaining steps of evaporating the volatile solvent (step 32); removing any excess plug material from the surfaces of the circuit board layer (step 34); and curing the plug material (step 36) are as described above for step 24, step 26 and step 28 respectively of Figure 2.

Figure 3 is a schematic perspective cross-sectional view of an embodiment of a circuit board layer 100 with a conductive plug 116 formed in a via 112 defined by the circuit board layer 100 in accordance with the present invention. The circuit board layer 100 has a first surface 104, a second surface 108, and defines at least one via 112 passing through the circuit board layer 100. The circuit board layer 100 may be a double sided, a multilayer or a rigid-flex circuit board layer. The circuit board layer 100 may be printed or unprinted. Optionally, the circuit board layer 100 may further comprise a base or pad (not shown) disposed along the circumference of the via on both the first surface 104 and the second surface 108 of the circuit board layer 100. These pads typically serve to facilitate connection of the conductive material contained in the via to a signal layer or electronic device. The via 112 contains a conductive plug 116.

Figure 4 is a schematic perspective cross-sectional view of an embodiment of a circuit board layer 200 having a first surface 204, a second surface 208, and a via 212 defined by the circuit board layer 200. The circuit board layer 200 may be a double sided, a multilayer or a rigid-flex circuit board layer. The circuit board layer 200 may be printed or unprinted. The via 212 has a pair of pads 220, 222 formed around its circumference upon both the first surface 204 and the second surface 208 respectively of the circuit board layer 200. These pads typically serve to facilitate connection of the conductive material 224 contained in the via to a signal layer or electronic device. The via 212 is plated with a conductive material 224 in order to provide for the transfer of electrical signals between the first surface 204 and the second surface 208 of the circuit board layer 200. Typically the via is plated with copper, but other conductive materials may also be used in accordance with the present invention.

The via 212 also contains a non-conductive plug 216. One advantage of having the via 200 filled with a non-conductive plug 216, is that the plug 216 prevents the passage of assembly materials through the via 212. Anther advantage is that the plug 216 allows for vacuum hold down of the circuit board for testing. Yet another advantage of the plug 216 is that it serves to strengthen the circuit board layer 200.

An apparatus may be used in accordance with the present invention in order to facilitate the filling of one or more vias in a circuit board. This apparatus allows the air in the vias to be replaced by a plug material in a volatile solvent. The apparatus of the present invention is referred to as a fixture and may be used with a stencil using standard screen printing techniques.

Figure 5 is a schematic cross-sectional side view of an embodiment of a fixture 318, holding a circuit board layer 300, and a stencil 360 in accordance with the present invention. The fixture 318 consists generally of a planar template 320, an air permeable layer 324, and a registration device 328. The planar template 320 has a first surface 332, a second surface 336, and one or more through-holes 340 passing through the template.

The template 320 may be made out of a sheet material with a thickness that is preferably greater than the thickness of the of the circuit board layer 300, so that air present in the via prior to filling may be easily displaced by plug material. For example, a 0.125 inch thick clear acrylic sheet or similar material may be used to form a template for a 0.06 inch thick circuit board in accordance with the present invention.

The through-holes 340 defined by the template 320 correspond in position to the one or more of the vias 312 defined by the circuit board layer 300 which are to be flooded with the plug material (not shown). The through-holes 340 should be larger in diameter than their corresponding vias 312 in the circuit board layer 300 so that a slight misalignment of the circuit board layer 300 and the template 320 will not cause the vias 312 to be only partially filled when flooded with plug material. Preferably, the diameters of the through-holes 340 are from about 10 mils to about 60 mils larger, more preferably from about 20 to about 50 mils larger, and most preferably are about 20 mils larger, than the diameters of the corresponding vias 312 in the printed circuit board layer 300. The through-holes 340 may be formed in the template 320 by etching, punching or drilling through the template.

The air permeable layer 324 is disposed on the second surface 336 of the template 320. The air permeable layer 324 may be a mesh screen, like a monofilament screen, a membrane or any other layer that will allow the passage of air through the layer. Preferably, the air permeable layer 324 is also substantially impermeable to the plug material, thus serving to protect the print table and any other equipment or material in the vicinity of the fixture 318 from contamination by plug material. For example, if the air permeable layer is a mesh screen, a mesh size of about 20 threads per inch to about 60 threads per inch may be used. Preferably a mesh size from about 25 thread per inch to about 30 threads per inch is used. Preferably the air permeable layer 324 is made from a material that is not degradable by the volatile solvent or any other solvent that may contact the mesh, for example, any cleaning solvents remaining on the circuit board from

previous processing steps. For examples, a monofilament polyester mesh may be used in accordance with the present invention.

A registration device 328 may be used to align the circuit board layer 300 with the fixture 318 so that the one or more vias 312 of the circuit board 300 to be filled with plug material are aligned with their corresponding through-holes 340 in the template 320. This registration device 328 may be one or more registration pins attached to the first surface 332 of template 320 as shown. Alternatively, the registration device may be affixed to a printing table or the second surface 308 of the circuit board layer 300. For example, registration pins may extend upwardly out of a printing table, through the fixture entirely, and into the circuit board layer. Many equivalent registration devices are well-known in the art and may be used in accordance with the present invention. The entire fixture 318 may be held together with adhesive or adhesive tape.

When the circuit board layer 300 is disposed upon and aligned with the fixture 318, and the circuit board layer 300 is flooded with plug material, the through-holes 340 in the template 320 allow the air in the vias 312 to be displaced by the plug material, and the air permeable layer 324 allows air passage out of the fixture 318. In a preferred embodiment, the air permeable layer 324 substantially prevents any plug material that may fall through the throughholes 340 defined by the template 320 and onto the air permeable layer 324, from passing through the air permeable layer 324 and out of the fixture 318, thus avoiding possible contamination of any surrounding equipment. The fixture 318 may also include a backing or support member 344 which supports the air permeable layer 324 and the template 320. This backing 344 may be made from material of any thickness, for example, a sheet of 0.250 inch thick polypropylene or similar flat stock.

A stencil 360 may be placed over the first surface 304 of the circuit board layer 300 prior to the step of filling the one or more vias 312 of the circuit board layer 300 with plug material. The stencil 360 has a first surface 378, a second surface 380, and defines one or more through-holes 364 which correspond in position with the one or more vias 312 in the circuit board layer 300 to be filled with plug material. The stencil 360 is typically a thin stainless steel sheet and the through-holes 364 are typically etched or drilled into and through the stainless steel sheet.

The through-holes 364 of the stencil 360 may be larger in diameter than their corresponding vias 312 in the circuit board layer 300. Preferably, the diameters of the through-holes 364 are from about 2 mils to about 6 mils larger, and more preferably are 4 mils larger, than the diameter of the corresponding vias 312 in the printed circuit board layer 300. The stencil 360 is generally about 3 mils to about 10 mils thick, preferably about 4 mils to about 8 mils thick.

The stencil 360 is normally held in a fixed position relative to a print bed, for example, by a clamp. The circuit board layer 300 and the fixture 318 may be aligned with the stencil 360 by manually aligning the through-holes 364 of the stencil 360 with the vias 312 of the circuit board layer 300. Alternatively, any registration device common to screen printing machines or tables might be used to align the stencil 360 with the circuit board layer 300 and the fixture 318.

The stencil 360 may be separated from the circuit board layer 300 by an off-contact distance. This off-contact distance may be from about $^1/_8$ inch to about $^3/_4$ inch, preferably from about $^2/_8$ inch to about $^3/_8$ inch in distance. The off-contact distance is important to reduce smear upon the first surface 304 of the circuit board layer 300. Smear may occur if the second surface 380 of the stencil 360 is contaminated with plug material and comes into contact with the first surface 304 of the circuit board layer 300.

The one or more vias 312 in the circuit board layer 300 may be filled by pushing plug material in a volatile solvent across a first surface 378 of the stencil 360. The material may be pushed across the stencil 360 with a squeegee 368. The squeegee may be constructed from rubber, metal, wood or the like. Preferably, the squeegee is constructed from rubber. The squeegee 368 may be passed across the surface 378 of the stencil 360 several times in order to effect the filling of the vias 312. Generally, the squeegee 368 is passed across the first surface 378 of the stencil 360 about 2 to 3 times for every 0.030 inch thickness of the circuit board layer. For example, about 4 to 6 squeegee strokes will be required for a circuit board layer that is 0.060 inches thick. Preferably, the squeegee is pushed across the first surface 378 of the stencil 360 at an angle α of from about 20° to about 80° with the first surface 378 of the stencil 360. Pushing the squeegee, as opposed to pulling the squeegee, and the angle between the end of the squeegee 368 in contact with the first surface 378 of the stencil 360, and the surface 378 of the stencil 360, is unique to this type of screen printing, increases the hydrostatic pressure of the plug material as

it is pushed across the surface of the stencil by the squeegee, and works particularly well with the method and apparatus of the present invention.

One advantage of the using the fixture 318 and the techniques described above, is that generally, a vacuum is not required in order to fill the vias 312 of the circuit board layer 300. Because typically, vacuum apparatus is costly and requires specialized equipment, this represents a significant cost savings.

However, a vacuum assist (not shown) may be used to fill the one or more vias 312 of the circuit board layer 300 with plug material. The vacuum assist may be attached to the fixture to create a negative pressure in the space defined by the through-holes 340 in the template 320 and the air permeable layer 324. The pressure should be high enough to flood the vias 312 of the circuit board layer 300 with plug material, but not high enough to empty the one or more vias 312 of the plug material once flooded. For example, the vacuum assist might be attached to the air permeable layer 324 so that it draws air out of the fixture through the air permeable layer. Alternatively, the fixture 318 may be placed upon a vacuum table such that the air permeable layer 324 is disposed directly upon the vacuum table.

Figure 6 is a flowchart diagram illustrating a method of forming a subassembly comprising a circuit board layer, the circuit board layer having one or more plugs formed therein, in accordance with the present invention. The method includes, in overview, the steps of: providing a circuit board layer, the circuit board layer having a first surface and a second surface, and defining a via containing a plug material in a volatile solvent (step 400); evaporating the volatile solvent (step 410); curing the plug material (step 420); laminating the circuit board layer to two sheets of conductive material with two intermediate layers of prepreg material (step 430).

Steps 400, 410 and 420 are as described above for Figure 1. In step 430, the circuit board layer is laminated to two sheets of conductive material with two intermediate layers of prepreg material. The conductive material may be copper foil. Alternatively the conductive material may be silver, gold, or any other conductive foil. The conductive sheet material may or may not be the same as the circuit board layer plating material. Preferably, the conductive sheets and the circuit board layer plating are copper. As described earlier, the circuit board layer may be printed or unprinted.

Prepreg materials are known in the art and typically comprise glass cloth impregnated with partially cured, or B-stage, epoxy resin. For example, the prepreg material sold under the trade name FR402 by Allied Signal (Morristown, NJ) is suitable for use in the present invention. When the above materials are laminated in step 430, the partially cured epoxy resin is further cured and adheres the sheets of conductive material to the circuit board layer. Lamination typically is carried out using a vacuum assisted lamination press where the layers to be laminated are assembled and exposed to pressures of about 200 psi and temperatures of about 350°F for about 2 hours. These conditions will be sufficient to form a laminate with most prepreg materials. For example, the FR402 prepreg material may be suitably cured by subjecting the subassembly to temperatures of about 350° F and about 200 psi for about 2 hours.

Figure 7 is a schematic perspective cross-sectional view of an embodiment of a subassembly 502 comprising a circuit board layer 501 having one or more plugs formed therein in accordance with the present invention. The subassembly 502 includes a circuit board layer 501 from which two pads 520, 522 have been etched. The circuit board layer is a dielectric material layer that initially is plated with conductive material, such as copper. The pads are defined by etching away the conductive plating, typically using a develop, etch and strip technique. The circuit board layer 501 defines a via 512. The via may be defined by laser drilling, mechanized drilling, chemical etching or punching the circuit board layer. The via is plated with a conductive material 524 and filled with plug material 516. The conductive material and plug material are as described above for Figures 1-6. Two sheets of conductive material 586 and 588 are laminated to the circuit board layer 501 with two intermediate layers of prepreg material 582, 584. The conductive material and the prepreg material and method of lamination are described above for Figure 6. A printed circuit board (not shown) may then be formed incorporating subassembly 502.

One advantage to having the via 512 filled with plug material 516 is that the resin in the two intermediate sheets of prepreg material 582, 584 cannot flow into the via 512 during lamination. This loss of prepreg resin from the prepreg material layers 582, 584 into the via 512 typically causes dimpling in the conductive layers 586, 588 of the subassembly 502. Planarity in the conductive layers 586, 588 is desired as it facilitates further processing of the subassembly. For example, if the surface of a conductive layer is to be developed, etched and stripped and that

surface is not planar, the photoresist may not conform to the surface properly, resulting in defects in the resulting traces.

Figure 8 is a flowchart diagram illustrating a method of forming a subassembly for use in a printed circuit board in accordance with the present invention. The method includes, in overview, the steps of: providing a subassembly comprising a circuit board layer laminated to two sheets of conductive material with two intermediate sheets of prepreg material (step 600); forming a via in the subassembly (step 610); plating the via (step 620); filling the via with a plug material in a volatile solvent (step 630); evaporating the volatile solvent (step 640); and curing the plug material (step 650).

In step 600, a subassembly is provided. As in Figure 1, the circuit board layer may be a double sided, multilayer or rigid-flex circuit board. The circuit board layer may be printed or unprinted. It is laminated to two sheets of conductive material with two intermediate sheets of prepreg material.

As described above for Figures 6 and 7, the conductive material may be copper, silver, gold, or any other conductive material and may or may not be the same as the circuit board layer plating material. Prepreg materials are known in the art and typically comprise glass cloth impregnated with partially cured, or B-stage, epoxy resin. When the above materials are laminated, the prepeg material is further cured and adheres the sheets of conductive material to the circuit board layer.

In step 610, a via is formed in the subassembly. The via may be formed by laser drilling, mechanized drilling, chemical etching or punching the subassembly to form the via using methods known in the art. In step 620, the via is plated. Typically, the via is plated with copper, but other conductive materials such as silver and gold may also be used.

In step 630, the via is filled with a plug material in a volatile solvent using materials and methods described above in connection with Figures 1-7. In step 640, the volatile solvent is evaporated as described above. Finally, in step 650, the remaining plug material cured as described above.

Figure 9 depicts a schematic perspective cross-sectional view of an embodiment of a subassembly 728 for use in a printed circuit board (not shown) in accordance with the present invention. The subassembly 728 includes a circuit board layer 700, two sheets of conductive

material 732, 736, two intermediate sheets of prepeg material 740, 744, a via 712, plating 724 and plug material 716.

The circuit board layer 700 includes a dielectric material layer 701 plated with two layers of conductive material 721, 723. Alternatively, the circuit board layer 700 might be printed to define circuitry (not shown). The circuit board layer 700, the two sheets of conductive material 732, 736 and the two intermediate sheets of prepreg material 740, 744 are laminated to form a subassembly 728. The subassembly 728 defines a via 712 passing through the subassembly 728. The via 712 is plated with a material 724 that typically is conductive to facilitate connection the transfer of electrical signals from the first surface 704 of the subassembly 728 to its second surface 708. Typically, the via 712 is plated with copper, but other conductive materials may be used in accordance with the present invention. The via 712 also contains a plug material 716, which may be conductive or non-conductive. The plug 716 may also be thermally conductive. A printed circuit board may be formed from the combination of a subassembly 728 as described above with either another subassembly and/or other circuit board layers. The materials and methods for making the assembly 728 are as described above for Figures 1-8.

One advantage of having the via 712 filled, is that the plug 716 prevents the passage of assembly materials though via 712 in further processing steps such as, for example, lamination to a second subassembly made in accordance with the method described for Figure 8. For example, if a subassembly 728 is laminated to a second subassembly or another circuit board layer with an intermediate sheet of prepreg material, the prepreg resin will not pass through the via 512. This is advantageous because resin loss may lead to insufficient adhesion. Another advantage is that the prepreg resin or other materials cannot pass through the via 512 and contaminate the outer surface of the subassembly 528 during lamination. Since during lamination the prepreg resin is further cured, any prepreg on the outer surface of the subassembly 528 would be cured to the surface. This would be undesirable because removal of the cured resin from the outer surface of the subassembly typically requires significant alteration of the surface of the subassembly to remove it.

Optionally, after lamination of the subassembly 728 to a second subassembly or circuit board layer, vias also may be formed in this new laminate (not shown). These vias optionally may be plated, filled with plug material in a volatile solvent, the solvent evaporated and the plug

material cured as described above. In this way, several subassemblies may be combined and laminated to form a multilayer printed circuit board.

Figure 10 is a flowchart diagram illustrating a method of forming a partially filled via in a circuit board layer in accordance with the present invention. The method includes, in general overview, of: providing a circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via (step 800); filling a portion of the via with a plug material in a volatile solvent (step 810); evaporating the volatile solvent (step 820); and curing the plug material to form a partially filled via (step 830).

Steps 800, 820 and 830 are as described above. Step 810 is as described above with the exception that the via is only partially filled with the plug material in volatile solvent. This may be achieved by varying the number of times the material is pushed across the stencil with a squeegee and/or the angle of the squeegee. For example, about 1 to about 4 squeegee strokes at an angle α of from about 20° to about 80° with the stencil surface, preferably from about 50° to about 70° with the stencil surface, are sufficient for a circuit board layer which is 0.060 inches thick. The resulting plug does not extend all the way through the via as shown and described below in Figure 11.

Figure 11 is a perspective cross-sectional photograph of an embodiment of a circuit board layer with a plated via partially filled with plug material in accordance with the present invention. As can be seen, the plug material does not extend all the way though the plated via. While the top side of the plug is substantially planar with the top surface of the circuit board layer, the bottom side of the plug does not extend through the via. Instead, there is a portion of the via on the bottom side of the circuit board layer that is not filled with plug material. Preferably, the bottom side of the circuit board layer is used as the solder side of the circuit board layer. The term "solder side" commonly is used to refer to the side of the circuit board layer to which test pins are applied to test the board.

One advantage to this embodiment is that a test pin can easily make sufficient electrical contact with the pads without the additional step of plating the pads on the surface of the circuit board layer prior to testing. This is because the tips of the test pins typically are tapered in shape so that if the plug were planar with the surface, the pins could not easily come into electrical contact with the plating. This is particularly true where the plug material in non-conductive.

However, the partially filled via of the present invention allows the test pin to enter the via and thereby easily come into electrical contact with the plating.

Also shown in Figure 11 is that the plug material on the top side, commonly referred to as the "component side" of the circuit board layer, is substantially planar to the top surface of the circuit board layer. This is advantageous if components are attached to the pads on this surface because the planar surface minimizes solder reflow into the via.

A printed circuit board containing one or more circuit board layers containing partially filled vias may be formed in accordance with the present invention. Such a printed circuit board generally also will have minimized solder reflow into the via due to the planarity of the plug on the component side of the circuit board layers.

Figure 12 is a flowchart diagram illustrating a method of forming a circuit board layer having a thermally conductive plug in accordance with the present invention. The method includes, in general overview, of: providing the circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via containing a thermally conductive plug material in a volatile solvent (step 1000); evaporating the volatile solvent (step 1010); and curing the thermally conductive plug material (step 1020).

In step 1000, a circuit board layer is provided that defines a via containing a thermally conductive plug material in a volatile solvent. Suitable thermally conductive materials in volatile solvent are known in the art. For example, the polymer-based compound CB100 made by DuPont, Inc. is thermally conductive as well as being electrically conductive, and is suitable for use in the present invention. Also suitable for use in the present invention is the thermoset screen-printable fill paste identified by the trademark GP202® available from Asahi Chemical Industry Co., Ltd. (Japan). Both of the above-referenced compounds have a thermal conductivity expressed in Watts per milliKelvin of between about 2 W/mK and about 4 W/mK. Step 1010 and step 1020 are as described above for Figures 1-10. A printed circuit board may be formed that incorporates one or more circuit board layers that have thermally conductive plugs formed therein. Additionally or alternatively, a printed circuit board may be formed with one or more thermally conductive plugs formed in vias defined by the printed circuit board and extending all the way through the printed circuit board.

One advantage of including thermally conductive plugs in a printed circuit board or a circuit board layer is that they can be used to transfer thermal energy from a first surface of the

printed circuit board or circuit board layer to a second surface of the printed circuit board or circuit board layer. For example, thermal energy generated by high speed devices might be transferred through a plurality of thermally conductive plugs from the component side of a circuit board layer to power or ground planes. This may significantly reduce the cost of any equipment necessary to cool the printed circuit board, particularly where high speed devices are attached to the printed circuit board which can generate as much as 20 to 30 Watts. Such high speed assemblies include, for example, High Input/Output Ball Grid Arrays.

Optionally, a cooling fin, water pipe, or other heat dispersing element may be placed on the non-component side of the printed circuit board to transfer heat from the thermally conductive plug and dissipate it. The use of thermally conductive plugs may render the use of forced air cooling sufficient where water cooling would be necessary without the thermally conductive plugs.

Practice of the invention will be still more fully understood from the following examples, which are presented herein for illustration purposes only and should not be construed as limiting the invention in any way.

Example 1: Formation of a Non-Conductive Plug in a Circuit Board Layer

A circuit board layer was provided with a 0.062 inch thickness and with a via having a diameter of 0.012 inch. The via was plated with copper such that the diameter of the plated via was 0.010 inch. The circuit board layer was placed upon and aligned with a fixture according to the present invention. The fixture included a template with 0.061 inch through-holes formed therein, and a 25 thread per inch monofilament polyester air permeable layer. A 6 mil thick stainless steel stencil, with a through-hole having a 0.016 inch diameter formed therein, which corresponds in position to the via in the circuit board, was then visually aligned with the circuit board layer. The vias were then filled with HYSOL® SR1000 non-conductive solder mask by pushing the solder mask across the stencil with a squeegee in 4 passes at an angle of 60° with the stencil surface. HYSOL® SR1000 non-conductive solder mask is a non-conductive plug material in volatile solvent. No vacuum assist was necessary to completely fill the vias. The plug material was then dried for 60 minutes at 70°C. The plug material was then cured at 150°F for 60 minutes. A 90% void free plug was achieved.

Example 2: Formation of a Subassembly Including a Circuit Board Layer, the Circuit Board Layer Having a Plug Formed Therein

A non-conductive plug in a circuit board layer was formed as described in Example 1. This circuit board layer was then laminated to two sheets of half ounce copper foil with two intermediate sheets of epoxy-based prepreg material sold under the trade name FR402 by Allied Signal (Morristown, NJ). These materials were laminated in a vacuum assist lamination press at 350° F at a pressure of 200 psi for 2 hours. No dimpling in the surface of the two copper sheets was observed.

Example 3: Formation of a Subassembly with a Plug Formed Therein

A subassembly was formed by laminating a 0.062 inch thick circuit board layer and two sheets of half ounce copper foil with two intermediate sheets of epoxy-based prepreg material sold under the trade name FR402 by Allied Signal (Morristown, NJ). These materials were laminated in a vacuum assist lamination press at 350° F at a pressure of 200 psi for 2 hours. A via having a diameter of 0.012 inch was then formed in the subassembly by mechanical drilling with a 0.012 inch bit. The via was plated, filled with plug material in a volatile solvent, the volatile solvent was evaporated, and the plug material cured as described above in Example 1.

Example 4: Lamination of Two Subassemblies

Two subassemblies were made as described above for Example 3. These two subassemblies were then laminated to each other with an intermediate layer of epoxy-based prepreg material sold under the trade name FR402 by Allied Signal (Morristown, NJ). These materials were laminated using a vacuum assist lamination press at 350° F at a pressure of 200 psi for 2 hours. Good lamination between the subassemblies was observed.

Example 5: Formation of a Partially Filled Via in a Circuit Board Layer

A plug was formed in a circuit board layer as described in Example 1, except that the squeegee was passed across the stencil only once at an angle of 60° with the stencil surface. The solder mask did not fill the entire length of the via, leaving an unfilled portion on the side of the via opposite the stencil. When cured, the plug was substantially planar to the surface of the circuit board layer adjacent to the stencil and formed a recess on the opposite side of the circuit

board layer. This recess was 0.012 inches in depth at its deepest point. Test pins inserted into this recess were observed to make sufficient electrical contact with the via plating.

Prophetic Example: Formation of Thermally Conductive Plugs in a Circuit Board Layer

One hundred thermally conductive plugs will be formed in a circuit board layer as described above for Example 1, except that a thermally conductive paste will be used for the plug material in volatile solvent. The thermally conductive paste will be that identified by the mark trademark GP202® and available from Asahi Chemical Industry Co., Ltd. (Japan). A High Input/Output Count Ball Grid Array will be attached to the thermally conductive plugs with power and ground pins on the component side. It is expected that the thermal plugs will reduce the overall temperature on the component side of the circuit board layer by as much as 20° F by transfer of thermal energy to a conductive plane on the opposite side of the circuit board layer.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting of the invention described herein. Scope of the invention is thus indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced herein.

What is claimed is:

Claims

1. A method of forming one or more plugs in a circuit board layer comprising the steps of:

(a) providing a circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via containing a plug material in a volatile solvent;

(b) evaporating the volatile solvent; and

(c) curing the plug material.

2. The method of claim 1 wherein step (a) comprises providing the circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via containing a solder mask in a volatile solvent.

3. The method of claim 2 wherein step (a) comprises providing the circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via containing a polymer-based conductive material in a volatile solvent.

4. The method of claim 2 wherein step (a) comprises providing the circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via containing a dielectric material in a volatile solvent.

5. The method of claim 1 wherein step (a) comprises:

(a-a) providing the circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via having a first diameter; and

(a-b) filling the via with a plug material in a volatile solvent.

6. The method of claim 5 further comprising the step of placing the circuit board layer on a fixture prior to step (a-b), the fixture comprising:

a planar template, having a first surface, a second surface, and defining a through-hole having a second diameter and corresponding in position to the via defined by the circuit board layer; and

an air permeable layer disposed on the second surface of the template.

7. The method of claim 6 wherein the second diameter of the through-hole defined by the template is larger than the first diameter of the via defined by the circuit board layer.

8. The method of claim 6 wherein the air permeable layer is substantially impermeable to the plug material.

9. The method of claim 5 further comprising the step of placing a stencil over the first surface of the circuit board layer prior to step (a-b), the stencil having a first surface, a second surface, and defining a through-hole having a third diameter and corresponding in position to the via defined by the circuit board layer.

10. The method of claim 9 further comprising the step of aligning the through-hole defined by the stencil with the via defined by the circuit board layer.

11. The method of claim 9 wherein the stencil is separated from the circuit board layer by an off-contact distance.

12. The method of claim 9 wherein the third diameter of the through-hole defined by the stencil is larger than the first diameter of the via defined by the circuit board layer.

13. The method of claim 9 wherein step (a-b) comprises filling the via with a plug material in a volatile solvent by pushing the plug material across the first surface of the stencil with a squeegee.

14. The method of claim 13 wherein step (a-b) further comprises using a vacuum to assist filling the via with the plug material in the volatile solvent.

15. The method of claim 1 wherein step (b) comprises evaporating the volatile solvent at a controlled rate, such that the creation of one or more voids in the plug material is minimized.

16. The method of claim 1 further comprising the step of removing any plug material disposed on the first surface of the circuit board layer prior to step (c).

17. The method of claim 1 further comprising the step of removing any plug material disposed on the first surface and the second surface of the circuit board layer prior to step (c).

18. The method of claim 1 further comprising the step of removing any plug material disposed on the first surface and the second surface of the circuit board layer by brushing the first

surface and the second surface of the circuit board layer with a nylon roller brush prior to step (c).

19. A circuit board layer comprising one or more plugs formed by a method of forming the one or more plugs in the circuit board layer, comprising the steps of:

(a) providing the circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via containing a plug material in a volatile solvent;

(b) evaporating the volatile solvent; and

(c) curing the plug material.

20. A fixture for filling a via having a first diameter formed in a circuit board layer, the fixture comprising:

a planar template, having a first surface, a second surface, and defining a through-hole having a second diameter and corresponding in position to the via formed in the circuit board layer; and

an air permeable layer disposed on the second surface of the template.

21. The fixture of claim 20 further comprising a registration device disposed on the first surface of the template for aligning the circuit board layer with the template.

22. The fixture of claim 20 wherein the second diameter of the through-hole defined by the template is larger than the first diameter of the via defined by the circuit board layer.

23. The fixture of claim 20 wherein the air permeable layer comprises a mesh screen.

24. The fixture of claim 20 further comprising a vacuum assist.

25. A method of forming a subassembly comprising a circuit board layer, the circuit board layer having one or more plugs formed therein, the method comprising the steps of:

(a) providing a circuit board layer, the circuit board layer having a first surface and a second surface, and defining a via containing a plug material in a volatile solvent;

(b) evaporating the volatile solvent;

(c) curing the plug material; and

(d) laminating the circuit board layer to two sheets of conductive material with two intermediate layers of prepreg material.

26. A subassembly comprising a circuit board layer, the circuit layer having one or more plugs formed therein, formed by a method comprising the steps of:

(a) providing a circuit board layer, the circuit board layer having a first surface and a second surface, and defining a via containing a plug material in a volatile solvent;

(b) evaporating the volatile solvent;

(c) curing the plug material; and

(d) laminating the circuit board layer to two sheets of conductive material with two intermediate layers of prepreg material.

27. A method of forming one or more plugs in a subassembly for use in a printed circuit board comprising the steps of:

(a) providing a subassembly comprising a circuit board layer laminated to two sheets of conductive material with two intermediate sheets of prepreg material;

(b) forming a via in the subassembly;

(c) plating the via;

(d) filling the via with a plug material in a volatile solvent;

(e) evaporating the volatile solvent; and

(f) curing the plug material.

28. The method of claim 27 wherein step (e) comprises evaporating the volatile solvent at a controlled rate, such that the creation of one or more voids in the plug material is minimized.

29. The method of claim 27, further comprising the step of removing any plug material disposed on a surface of the subassembly prior to step (f).

30. The method of claim 27, further comprising the following steps of:

(g) forming one or more plugs in a second subassembly for use in a printed circuit board comprising the steps (a) through (f) above; and

(h) laminating the subassembly to the second subassembly with a third intermediate sheet of prepreg material.

31. A subassembly for use in a printed circuit board, formed by a method comprising the steps of:

(a) providing a circuit board laminate comprising a circuit board layer laminated to two sheets of conductive material with two intermediate sheets of prepreg material;

(b) forming a via in the circuit board laminate;

(c) plating the via;

(d) filling the via with a plug material in a volatile solvent;

(e) evaporating the volatile solvent; and

(f) curing the plug material.

32. A method of forming a partially filled via in a circuit board layer comprising the steps of:

(a) providing a circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via;

(b) filling a portion of the via with a plug material in a volatile solvent;

(b) evaporating the volatile solvent; and

(c) curing the plug material to form a partially filled via.

33. A circuit board layer comprising a partially filled via, the partially filled via having been formed by a method comprising the steps of:

(a) providing a circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via;

(b) filling a portion of the via with a plug material in a volatile solvent;

(b) evaporating the volatile solvent; and

(c) curing the plug material to form a partially filled via.

34. A method of forming a circuit board layer comprising a thermally conductive plug for transfer of thermal energy from a first surface of the circuit board layer to a second surface of the circuit board layer comprising the steps of:

(a) providing the circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via containing a thermally conductive plug material in a volatile solvent;

(b) evaporating the volatile solvent; and

(c) curing the thermally conductive plug material.

35. A circuit board layer comprising a thermally conductive plug for transfer of thermal energy from a first surface of the circuit board layer to a second surface of the circuit board layer formed by a method comprising the steps of:

(a) providing the circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via containing a thermally conductive plug material in a volatile solvent;

(b) evaporating the volatile solvent; and

(c) curing the thermally conductive plug material.

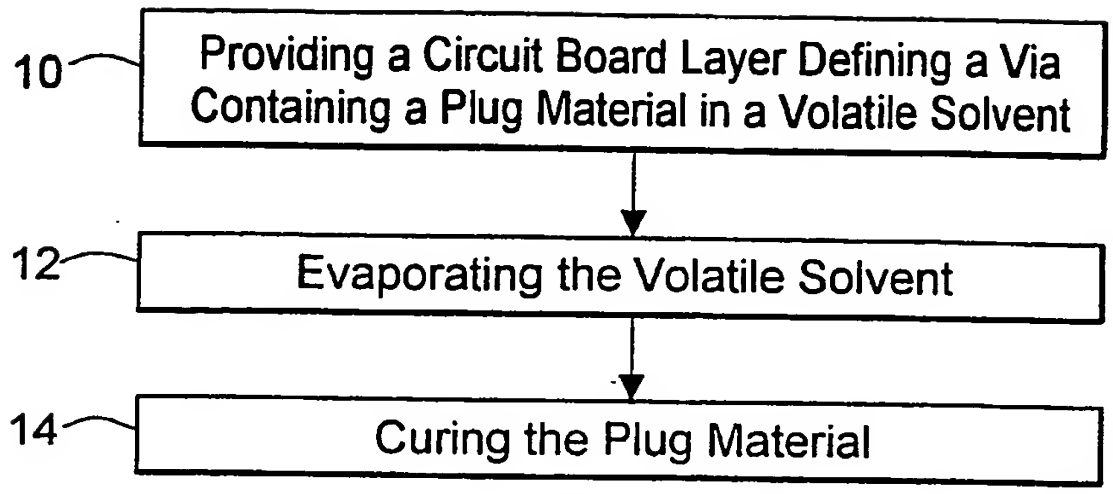

10
Providing a Circuit Board Layer Defining a Via Containing a Plug Material in a Volatile Solvent
12
Evaporating the Volatile Solvent
14
Curing the Plug Material

FIG. 1

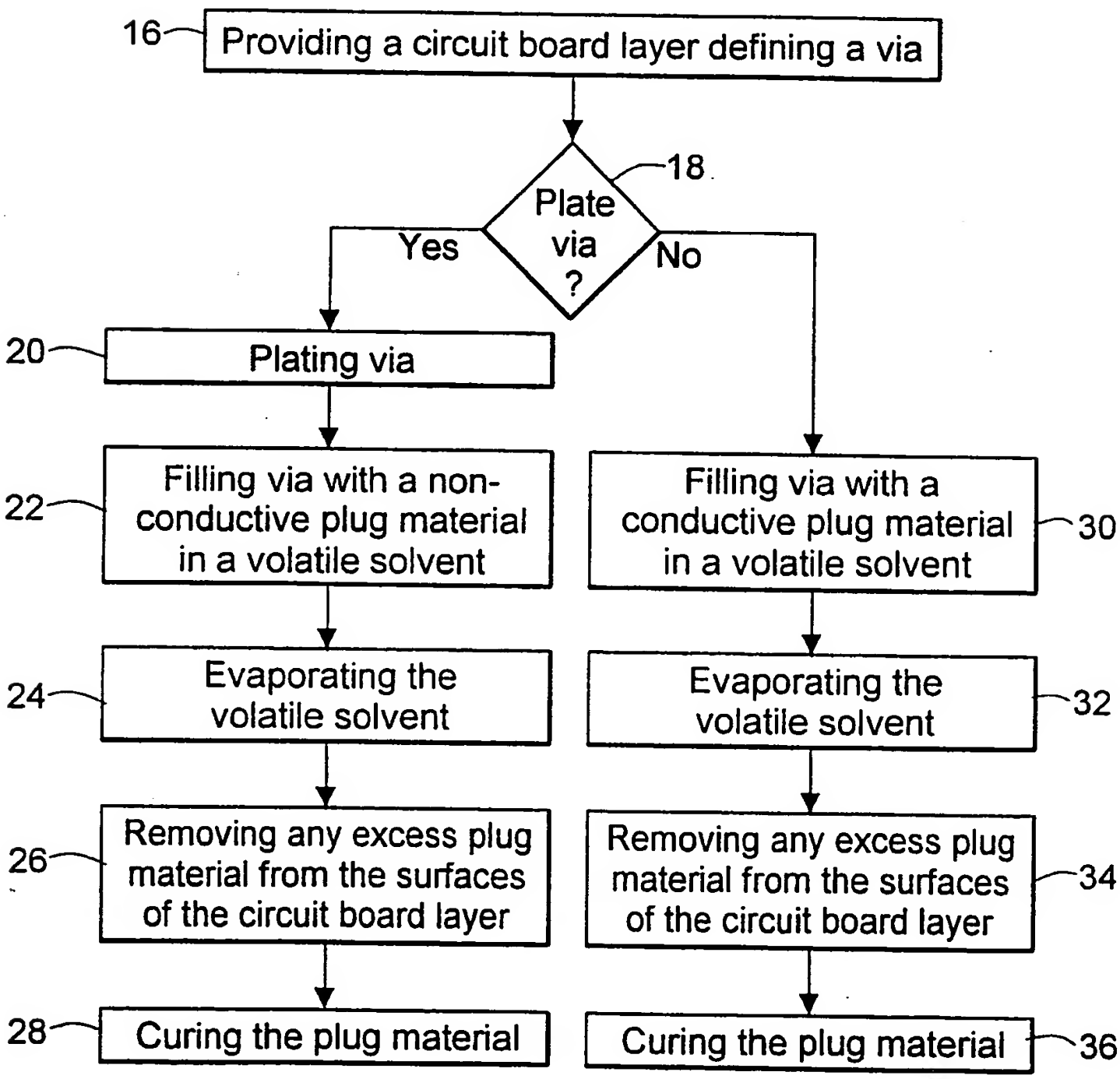

16
Providing a circuit board layer defining a via
18
Plate via ?
Yes
No
20
Plating via
22
Filling via with a non-conductive plug material in a volatile solvent
24
Evaporating the volatile solvent
26
Removing any excess plug material from the surfaces of the circuit board layer
28
Curing the plug material
30
Filling via with a conductive plug material in a volatile solvent
32
Evaporating the volatile solvent
34
Removing any excess plug material from the surfaces of the circuit board layer
36
Curing the plug material

FIG. 2

FIG. 3

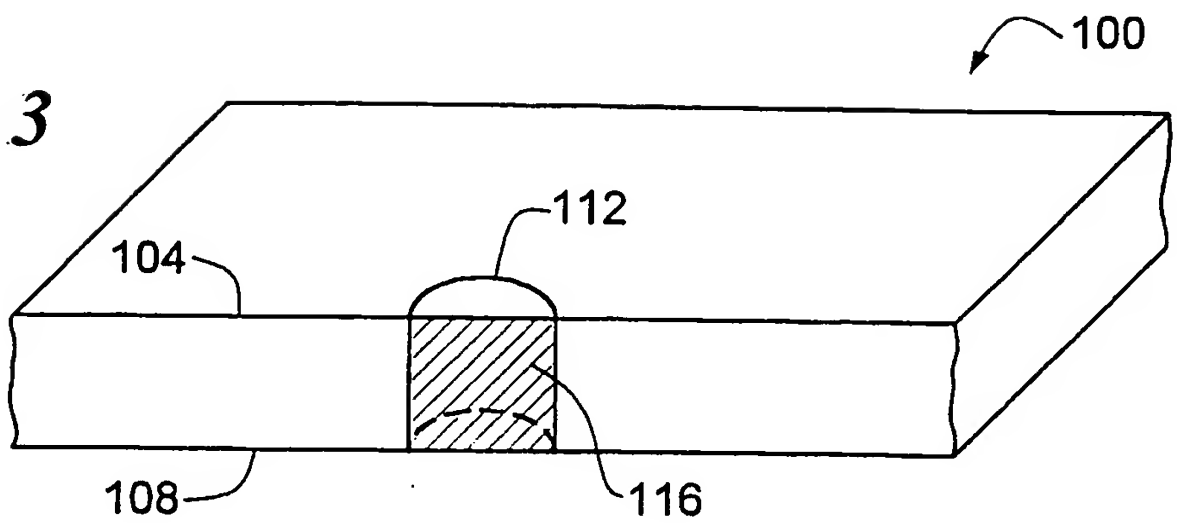
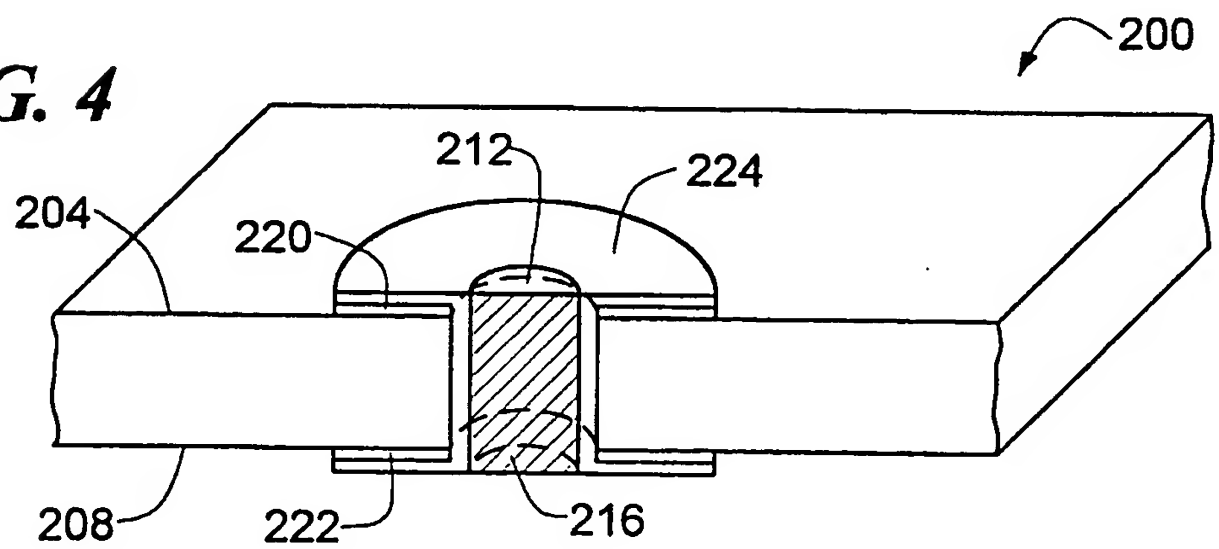


FIG. 4



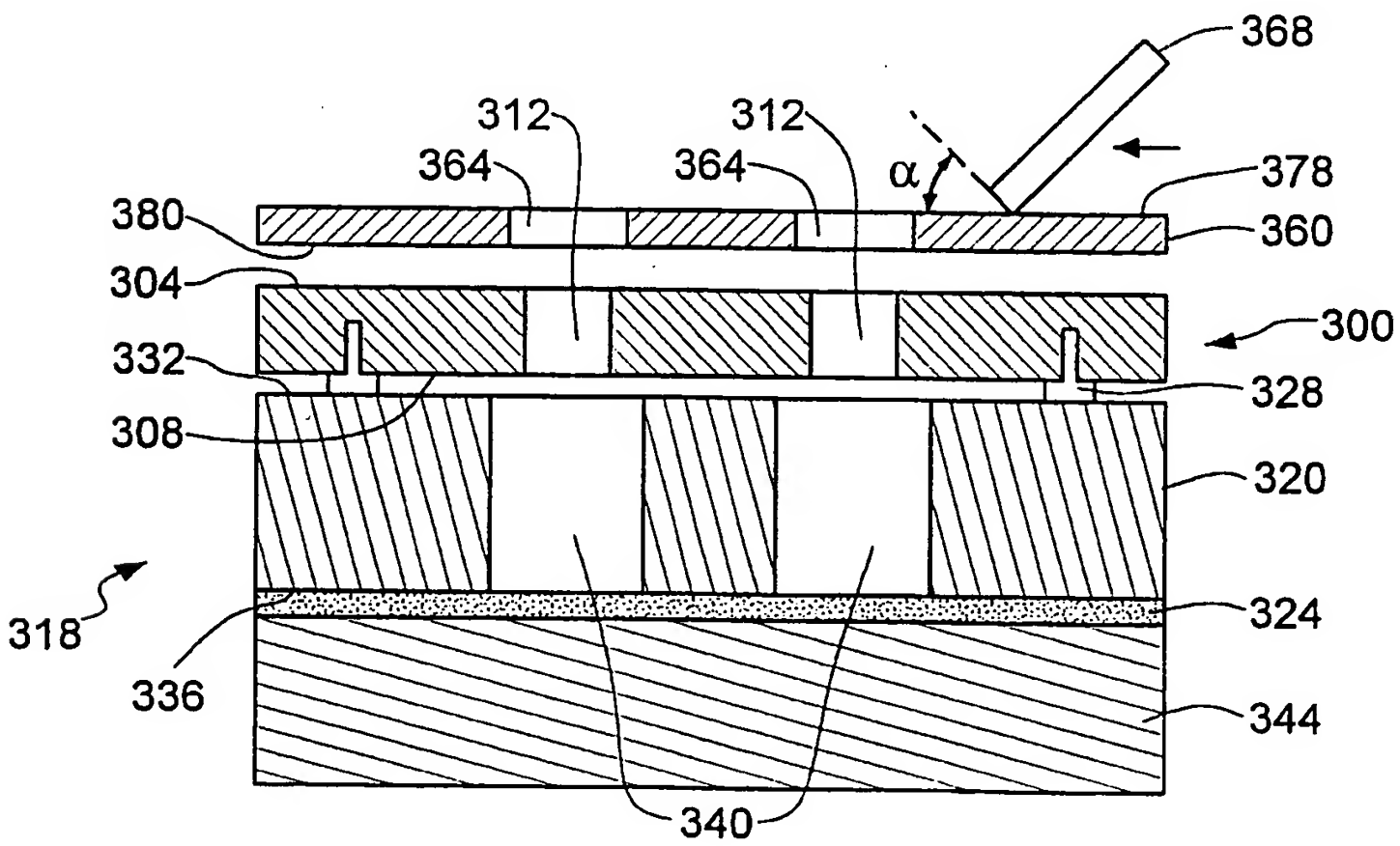


FIG. 5

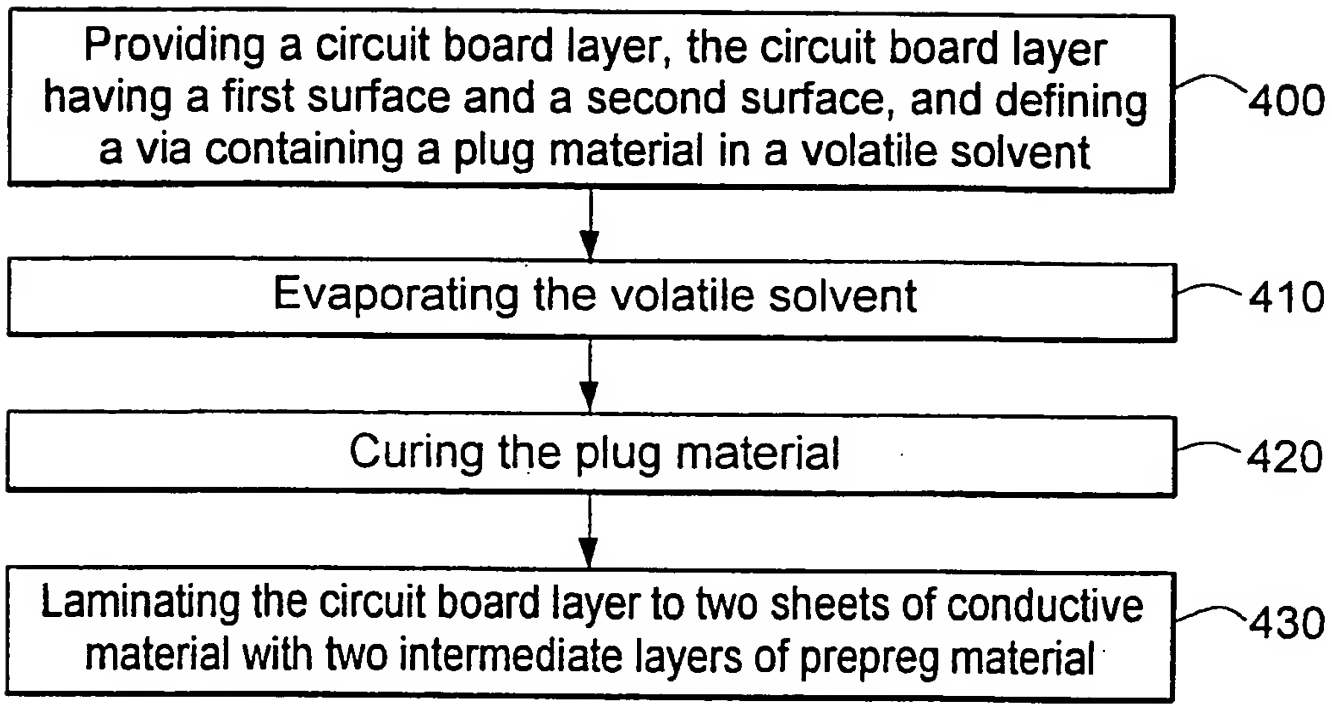

Providing a circuit board layer, the circuit board layer having a first surface and a second surface, and defining a via containing a plug material in a volatile solvent
400
Evaporating the volatile solvent
410
Curing the plug material
420
Laminating the circuit board layer to two sheets of conductive material with two intermediate layers of prepreg material
430

FIG. 6

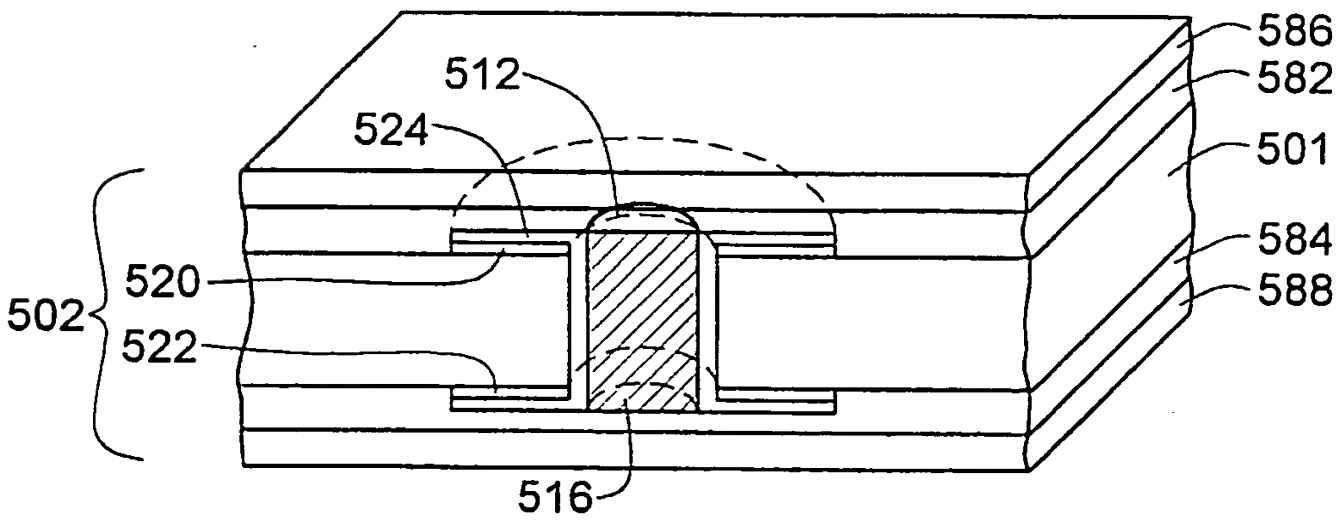

586
582
512
524
501
584
588
520
502
522
516

FIG. 7

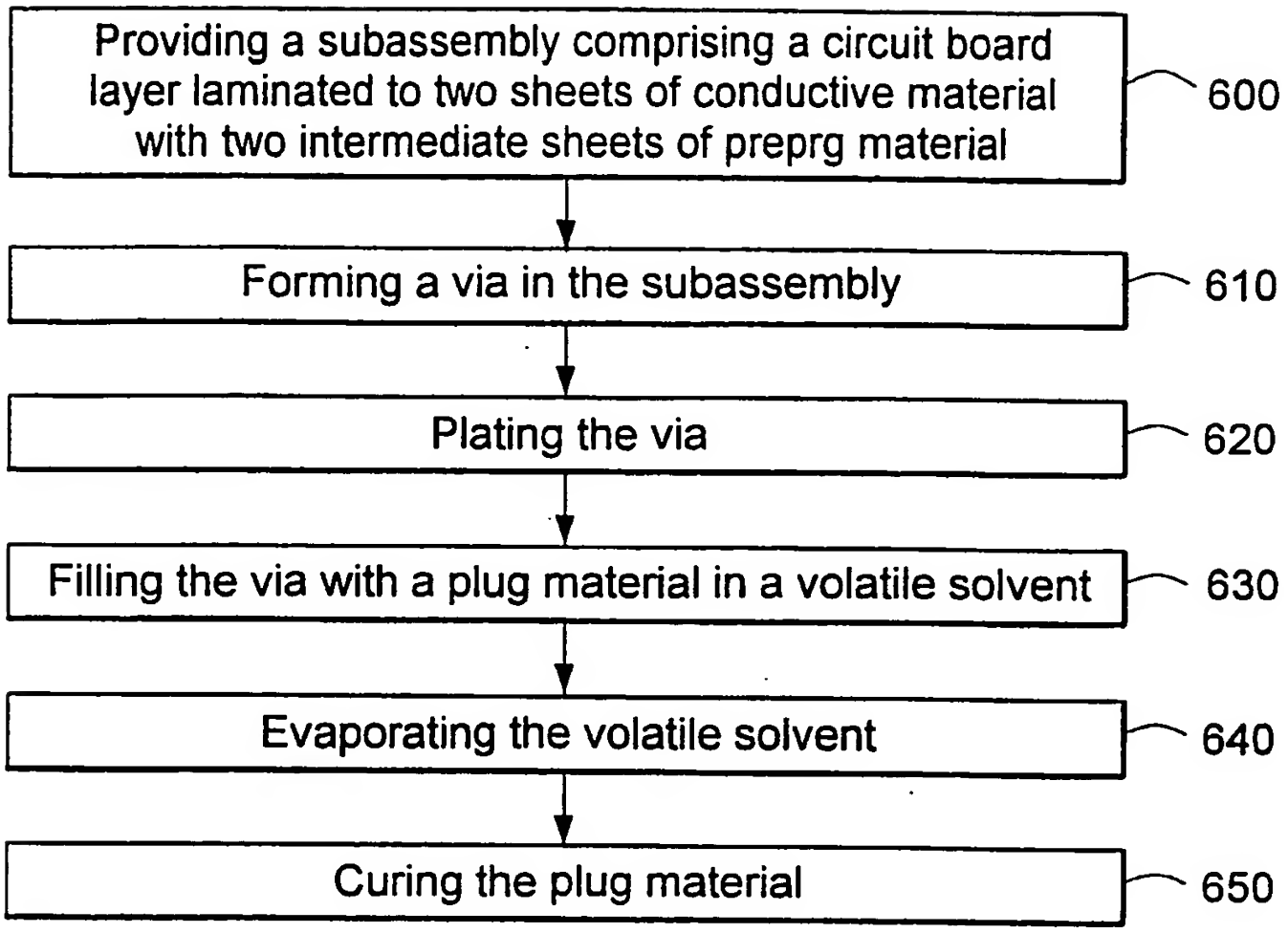

Providing a subassembly comprising a circuit board layer laminated to two sheets of conductive material with two intermediate sheets of preprg material
600
Forming a via in the subassembly
610
Plating the via
620
Filling the via with a plug material in a volatile solvent
630
Evaporating the volatile solvent
640
Curing the plug material
650

FIG. 8

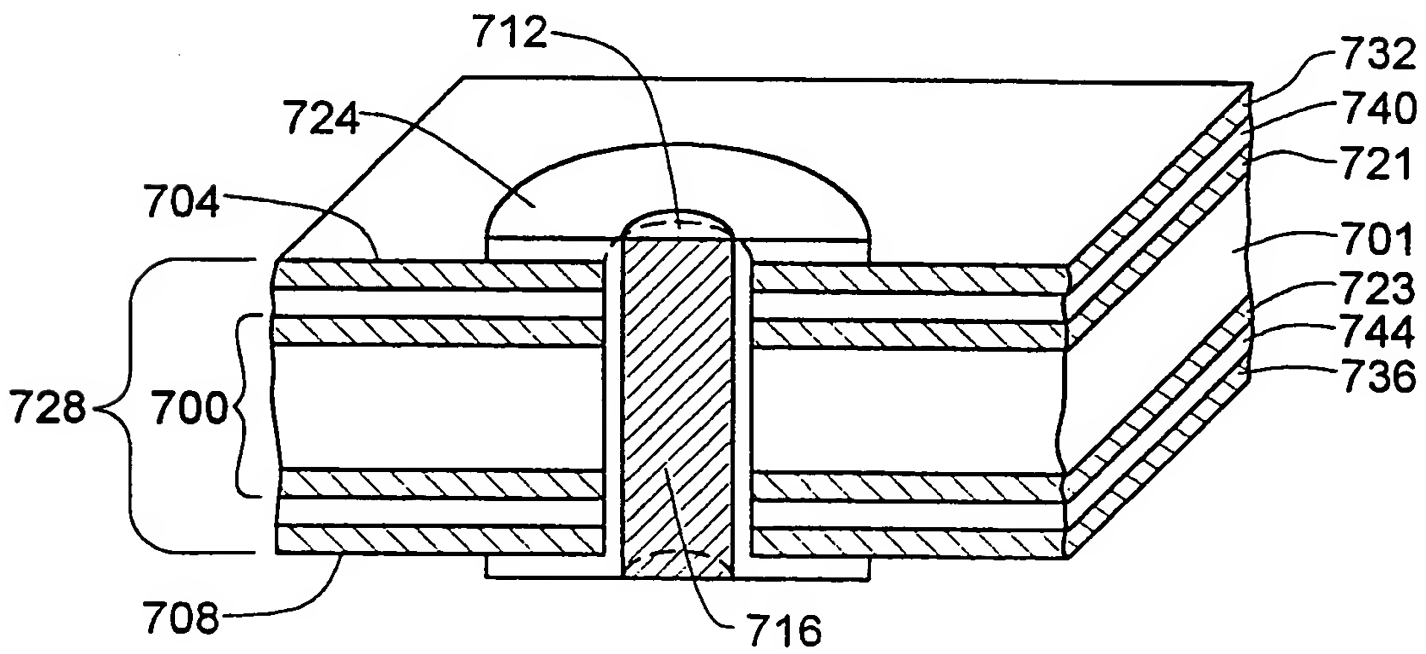

712
724
704
728
700
708
716
732
740
721
701
723
744
736

FIG. 9

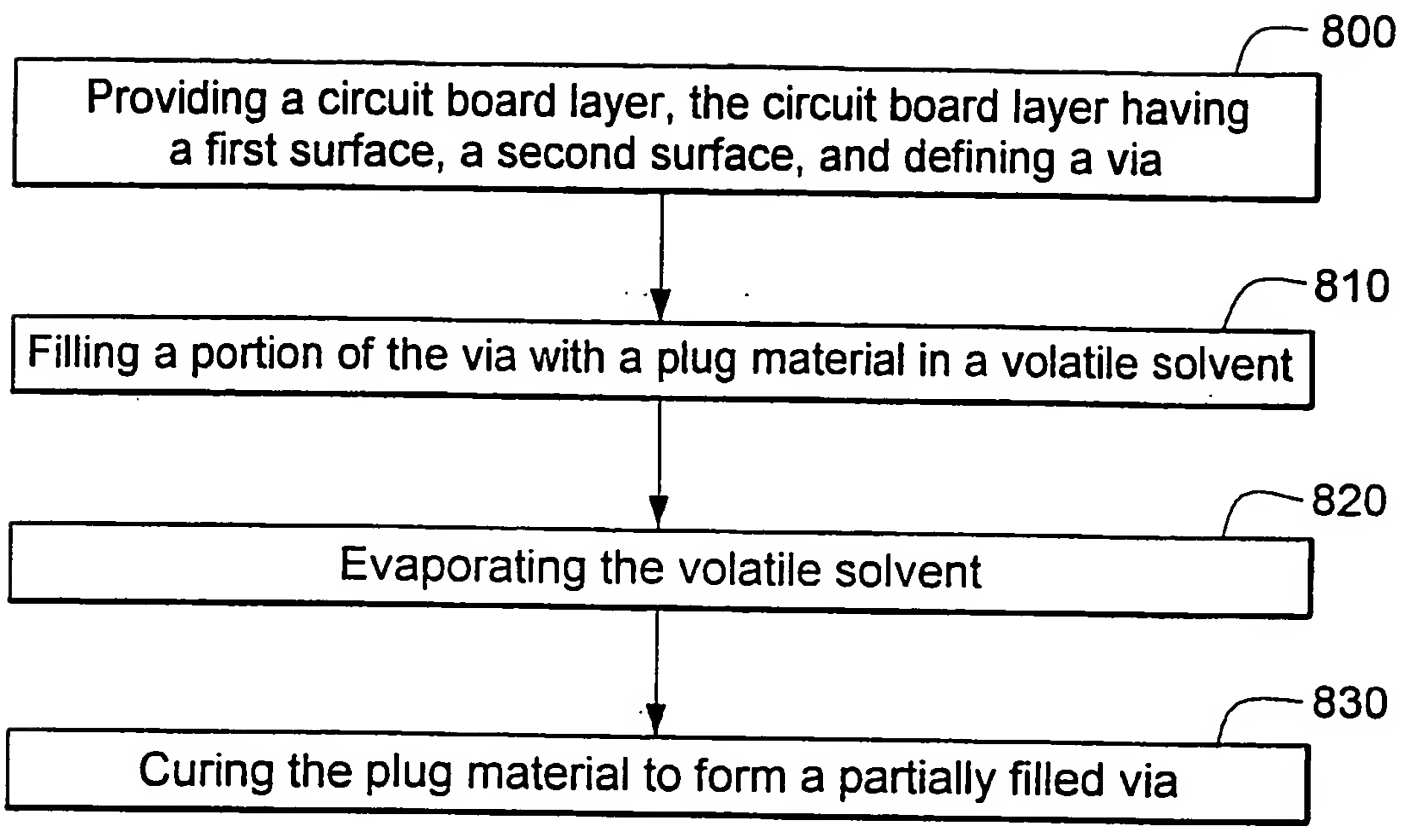

800
Providing a circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via
810
Filling a portion of the via with a plug material in a volatile solvent
820
Evaporating the volatile solvent
830
Curing the plug material to form a partially filled via

FIG. 10

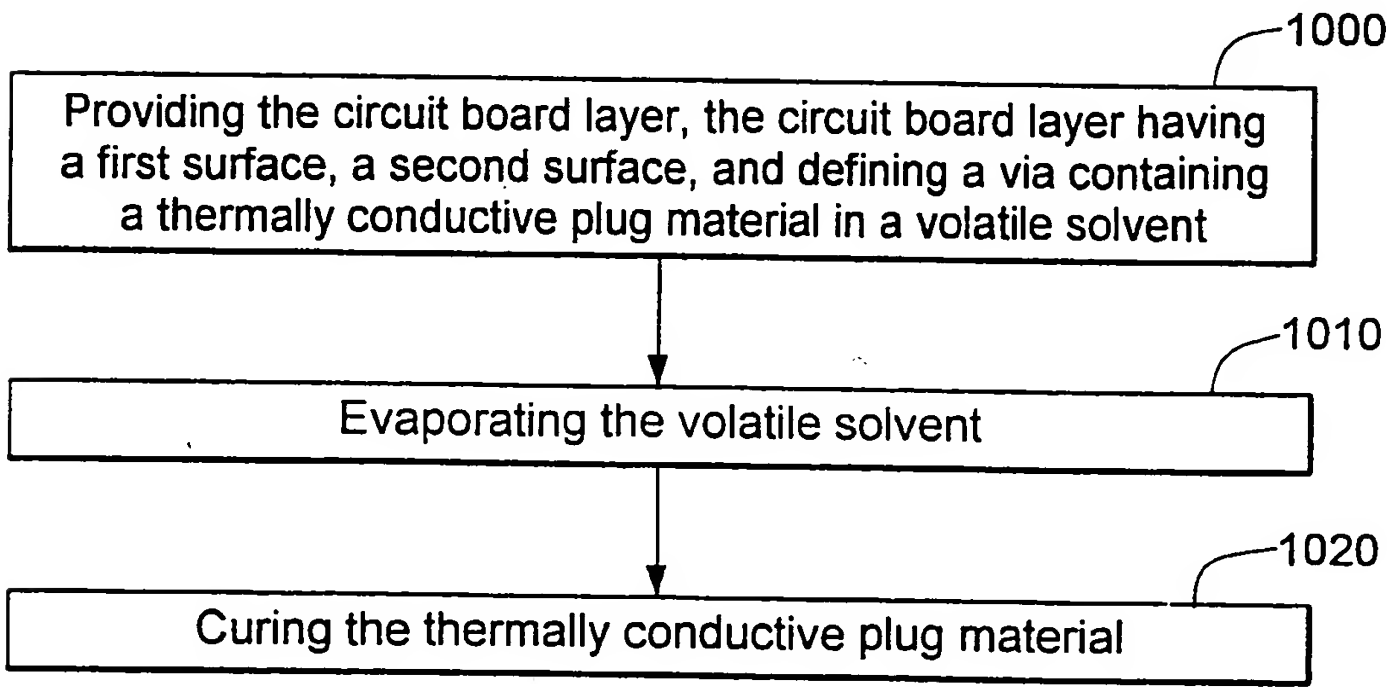

1000
Providing the circuit board layer, the circuit board layer having a first surface, a second surface, and defining a via containing a thermally conductive plug material in a volatile solvent
1010
Evaporating the volatile solvent
1020
Curing the thermally conductive plug material

FIG. 12

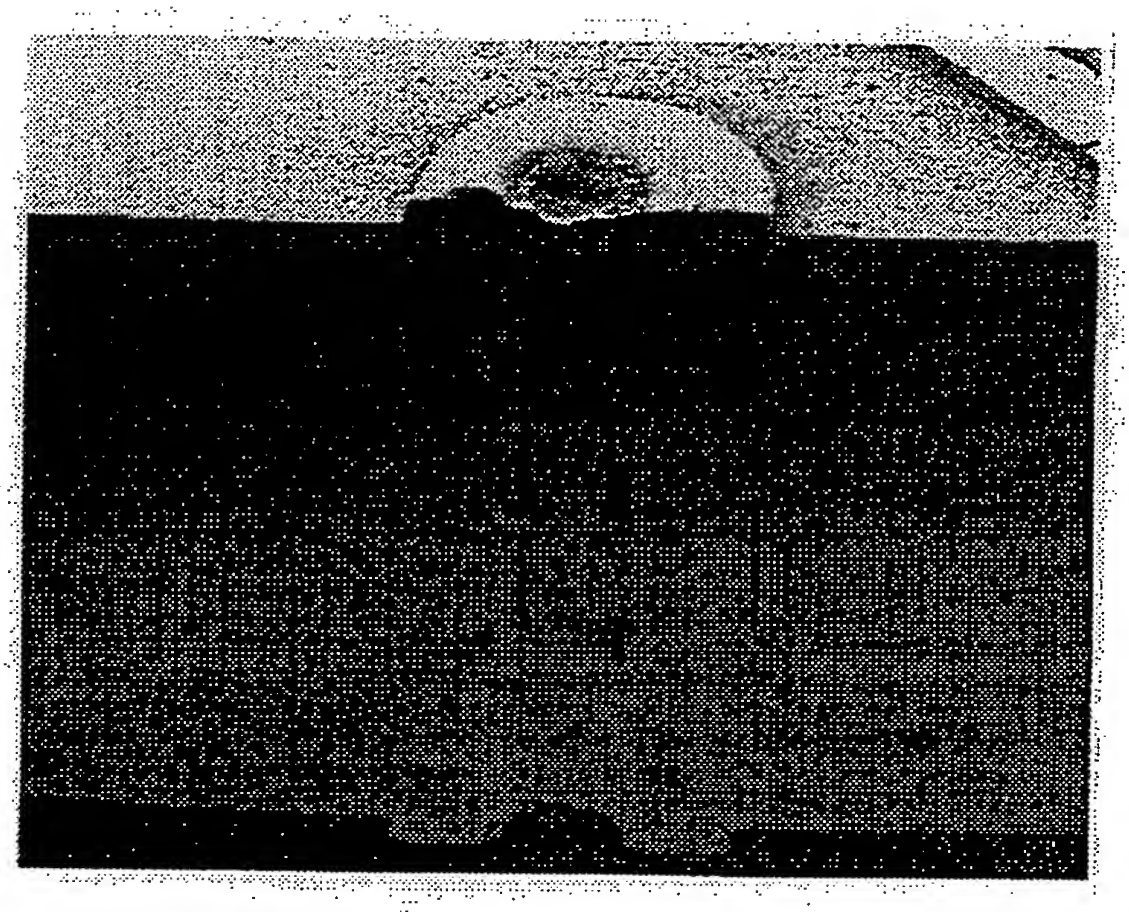


FIG. 11

INTERNATIONAL SEARCH REPORT

Inter: nal Application No
PCT/US 99/20245

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05K3/00 H05K3/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 86 06243 A (EIDENBERG) 23 October 1986 (1986-10-23) the whole document	1-5,9, 10, 12-14,19
A		6,7,20, 22,24
X	FR 2 684 836 A (LABORATOIRE ASSISTANCE PRODUCTION ET ENVIRONNEMENT L.A.P.E.) 11 June 1993 (1993-06-11) page 3, line 31 -page 4, line 9 page 5, line 4 - line 11 figures	1-5,19
Y		6-8,20, 22, 24-27, 30,31, 34,35

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search	Date of mailing of the international search report
2 December 1999	10/12/1999

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Inter ›nal Application No
PCT/US 99/20245

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 568 (E-861), 15 December 1989 (1989-12-15) & JP 01 236694 A (TOSHIBA CORP), 21 September 1989 (1989-09-21) abstract	1,5,9, 10,13, 14,19
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A	US 5 220 723 A (OKADA) 22 June 1993 (1993-06-22) column 3, line 2 - line 28; figure 2	1,3,5,19
Y		25-27, 30,31

Y	EP 0 723 388 A (MATSUSHITA ELECTRIC INDUSTRIAL CO.) 24 July 1996 (1996-07-24) abstract	34,35

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A	FR 2 714 567 A (THOMSON HYBRIDES) 30 June 1995 (1995-06-30) claims; figures	1,5,6,8, 13,14, 19,20, 24-26, 32,33

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